

PMC-APN007 Setting up LVR level

Setting up LVR level Application Note

Applied for: All PMC & PMS series MCU

1. 【LVR】

The frequency of SYSCLK must be considered when setting up the LVR. Generally, the faster is the SYSCLK, the higher is the LVR. In order to prevent the LVR from set up to be too low, IDE will check their relation between SYSCLK and LVR during the compiling. However, user can disable this checking against LVR through inserting "#pragma disable check_lvd" in any place of the program. Please notice that, disabling this checking does not represent the lowest working voltage of the IC becomes lower. If user set a too low LVR, IC may not reset and become malfunction if the VDD drops under the lowest working voltage limit. Therefore, user has to estimate and take his own risk to the consequences for disabling the checking in accordance with the practical application situation.

(1) 【Under_20ms_VDD_Ok】

There is a special code option in the IC: Under_20ms_VDD_Ok.

If the IC VDD can rise to normal operation voltage within 20ms during power-on, user can consider setting "Under_20mS_VDD_Ok "= YES. The LVR voltage can hence be adjusted one level further lower. This is applied for the case of battery supply and no bulk VDD capacitor existing. In contrast, for slow power-on case (such as using resistor-capacitor AC step down circuit or using bulk VDD capacitor), LVR must be set higher to avoid wrong operation due to high speed power-on in low voltage. In this case, please set "Under_20mS_VDD_Ok" = NO.

For slow power-on, user can use ILRC first and then execute IHRC/n once the power is stable.

.ADJUST_IC SYSCLK=ILRC, ...; // Watchdog Disable... ...; .delay nnn; // Please adjust accordingly ...; CLKMD = 0x34; // IHRC/2 = 8MIPS

2. The change of LVR setting will only alter the level of low voltage reset, but it will not alter the execution of the program.



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3. To change LVR

(1) Refer to "Execution" in IDE utility --> "Parameter of program" --> Open Code Option list, then choose LVR (which is displayed as "LVD" as below diagram) for the application. The diagram is shown as below :

ОК		Cancel
nder 20mS_VDD_Ok	LVD	FPPA
• No	C 4.0V	C 1-FPPA
Yes	○ 3.5V	© 2-FPPA
Security	C 2.75V	
Enable	○ 2.5¥	
Disable	C 1.8V	
	○ 2.2¥	
	C 2.0V	

(2) If LVR is set to be too low, an "ERROR" message will be displayed as below :

<u>.CHIP</u>	PMC232					
77{{PHD	.Code Option	Under 20mS	VDD OK	No		
	.Code Option	FPPA	2-FPPA			
	.Code_Option	LVD	3.OV		// Maximum	performance
1						
oject1\	Project1.PRE(4):	.Code_Optic	on : LVD is t	oo low.		

(3) If IC can rise to the normal operation voltage within 20 ms during power-on, user can choose LVR within one level lower through IDE utility : "Execution" --> "Parameter of program" --> Open Code Option list, then choose "Yes" in "Under_20mS_VDD_Ok". Please refer to below diagram :

ок		Cancel
der_20mS_VDD_0k	LVD	FPPA
No	○ 4.0V	C 1-FPPA
Yes	C 3 5V	© 2-FPPA
Security	C 2.75V	
Enable	○ 2.5¥	
Disable	C 1.8V	
	○ 2.2¥	
	C 2.0V	



(4) After finishing above selection, please click "OK", then the LVR will be changed successfully.

<u>.CHIP</u>	PMC232			
//{{PAD	AUK CODE OPTION			
	.Code_Option	Under_20mS_U	JDD_Ok	Yes
	.Code Option	FPPA	2-FPPA	
	.Code_Option	LVD	3.GV	
	.Code_Option	Security	Enable	
//}}PAD	AUK_CODE_OPTION			

(5) For data in details, please refer to "slow power-on" of the user manual in the IDE.



If you have further questions to the application, please consult to our agent at your nearest location or contact us at <u>fae@padauk.com.tw</u>.